

## PROTECTION CIRCUIT

### BACKGROUND OF THE INVENTION

#### Field of the Invention

5        The present invention relates to a protection circuit for protecting the FET or the like for control of the energization state of current to the inductive load, and more particularly to a protection circuit to be applied for power source control of the vehicle-mounted power distributor section in various  
10 kinds.

#### Background Art

Fig. 6 is a circuit diagram of the conventional protection circuit and circuit arrangement the protection circuit is  
15 applied. The protection circuit of this kind, as shown in Fig. 6, has a Zener diode 5 interposed between the gate and the drain of an FET 3 as an N-channel MOS transistor, a switch 9 interposed on a connection line between the gate and a charge pump circuit 7 as a gate-drive voltage supply source thereof, a first resistor  
20 11 interposed between the gate and the source of the FET 3 and a second resistor 13 interposed between the gate of the FET 3 and the switch 9, as a countermeasure to the surge voltage caused upon powering off the inductive load (e.g. motor) 1.

The switch 9 serves also as an on-off switch for the FET  
25 3. During driving the load 1, the switch 9 connects between

the FET 3 gate and the charge pump circuit 7 thereby turning on the FET 3. Meanwhile, when the load 1 is powered off, the switch 9 disconnects between the gate and the charge pump circuit 7 thereby turning off the FET 3. Consequently, during driving the load 1, the drive voltage outputted from the charge pump circuit 7 is supplied to the gate of the FET 3 through the switch 9 and resistor 13. This turns on the FET 3, thereby energizing the load 1 and driving the load 1. During powering off the load 1, the switch 9 disconnects between the FET 3 gate and the charge pump circuit 7. This turns off the FET 3 at a time the gate voltage goes below a threshold voltage. Due to turning off the FET 3, a negative surge is caused on the source potential of the FET 3 by an inductive counter electromotive force on the load 1. The negative surge pulls the gate potential toward the minus through the resistor 1. When the gate-to-drain voltage difference of the FET 3 exceeds the threshold voltage of the Zener diode 5, the FET 3 is brought into conduction between the gate and the drain through the Zener diode 5. A current flows from the drain to the source through the Zener diode 5 and resistor 11. When the gate-to-source voltage difference caused thereupon exceeds the threshold voltage, the FET 3 is turned on. The on-state of the FET is held until the gate-to-source voltage goes below the threshold value. Therefore, during on of the FET 3, the counter electromotive force on the load 1 is absorbed by the power supplied through

the FET 3.

Fig. 7 is a figure showing the manner of a surge current, etc., during powering off the load 1, in the circuit arrangement of Fig. 6. In Fig. 7, the graph G1 represents a change in time of a current  $I_L$  (see Fig. 6) flowing through the load 1 during powering off the load 1, in the circuit arrangement of Fig. 6 while the graph G2 represents a change in time of a source voltage  $V_s$  (see Fig. 6) of the FET 3 during powering off the load 1, also in the circuit arrangement of Fig. 6. Meanwhile, the graph G3 of Fig. 7 represents a change in time of a source voltage  $V_s$  during powering off the load 1 when the Zener diode 5 is removed, in the circuit arrangement of Fig. 6.

#### SUMMARY OF THE INVENTION

However, the conventional protection circuit involves a problem that the circuit arrangement is increased in size and cost because of using the Zener diode 5. Furthermore, there is also a problem that radio-frequency noise occurs when turning on/off the Zener diode.

Therefore, it is an object of the present invention to provide, while achieving to reduce the size and cost of circuit arrangement, a protection circuit that countermeasure can be taken to the surge voltage during powering off the load in a circuit arrangement the invention is applied wherein there is no need to use an element, such as a Zener diode, that causes

radio-frequency noise.

According to the first aspect of the invention, there is provided a protection circuit to be provided for a circuit arrangement having an inductive load and an FET as an N-channel MOS transistor provided upstream of the load with respect to a flow of power current, the FET controlling an energization state of the load, the protection circuit including a first connection changer interposed on a connection line between a gate of the FET and a gate drive voltage supply source, the first connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground.

According to the second aspect of the invention, there is provided a protection circuit to be provided for a circuit arrangement having an inductive load and an FET as an N-channel MOS transistor provided upstream of the load with respect to a flow of power current, the FET controlling an energization state of the load, the protection circuit including a first connection changer interposed between a portion on a first connection line and a ground, the first connection changer connecting and disconnecting between the portion and the ground. Preferably, the first connection line connects a gate of the FET and a gate drive voltage supply source.

According to the third aspect of the invention, there

is provided a protection circuit to be provided for a circuit arrangement having an inductive load and an FET as a P-channel MOS transistor, the FET for controlling an energization state of the load, the protection circuit including a connection  
5 changer interposed on a connection line between a gate of the FET and a ground, the connection changer changing a connection state between a first connection state in which the gate is connected to the ground and a second connection state in which the gate is connected to a source of the FET, a first resistor  
10 interposed between the gate of the FET and the connection changer or between the connection changer and the source of the FET, and a second resistor interposed between the gate and the drain of the FET.

According to the fourth aspect of the invention, there  
15 is provided a protection circuit to be provided for a circuit arrangement having an inductive load and an FET as a P-channel MOS transistor, the FET controlling an energization state of the load, the protection circuit including a connection changer interposed between a portion, on a connection line between a  
20 gate and a source of the FET, and a ground, the connection changer connecting and disconnecting between the portion and the ground, a first resistor interposed on a route of from the gate of the FET to the source thereof through the connection line, and a second resistor interposed between the gate and a drain of the  
25 FET.

According to the fifth aspect of the invention, there is provided a protection circuit to be provided for a circuit arrangement having an inductive load and an IGBT provided upstream of the load with respect to a flow of power current, the IGBT controlling an energization state of the load, the protection circuit including a connection changer interposed on a connection line between a gate of the IGBT and a gate drive voltage supply source, the connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground.

According to the sixth aspect of the invention, there is provided a protection circuit to be provided for a circuit arrangement having an inductive load and an IGBT provided upstream of the load with respect to a flow of power current, the IGBT controlling an energization state of the load, the protection circuit including a connection changer interposed between a portion on a connection line and a ground, the connection changer connecting and disconnecting between the portion and the ground. Preferably, the connection line connects a gate of the IGBT and a gate drive voltage supply source.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be more readily described with

reference to the accompanying drawings:

FIG. 1 is a circuit diagram of a protection circuit and a circuit arrangement the protection circuit is applied, according to a first embodiment of the present invention;

5        Fig. 2 is a figure showing a manner of a surge current, etc., during powering off a load in the Fig. 1 circuit arrangement;

10        Fig. 3 is a diagram showing a circuit further detailed of the protection circuit included in the Fig. 1 circuit arrangement;

Fig. 4 is a circuit diagram of a protection circuit and a circuit arrangement the protection circuit is applied, according to a second embodiment of the present invention;

15        Fig. 5 is a circuit diagram of a protection circuit and a circuit arrangement the protection circuit is applied, according to a third embodiment of the present invention;

Fig. 6 is a circuit diagram of a protection circuit and a circuit arrangement the protection circuit is applied, in the conventional; and

20        Fig. 7 is a figure showing a manner of a surge current, etc., during powering off a load in the Fig. 6 circuit arrangement.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25        Fig. 1 is a circuit diagram of a protection circuit and

circuit arrangement the protection circuit 20 is applied, according to a first embodiment of the present invention. The circuit arrangement, a protection circuit 20 of this embodiment is applied, has an inductive load (e.g. motor) 21, an FET 23  
5 as an N-channel MOS transistor for taking control of the energization state to the load 21, and a charge pump circuit (gate drive voltage supply source) for driving the FET 23, as shown in Fig. 1. The load 21 and the FET 23 are interposed in series on a conductor line 27 such that the FET 23 is positioned  
10 upstream with respect to the direction of power current flow. The conductor line 27 is interposed between the power line 29 and the ground. On the conductor line 27, a diode 31 is connected in series with the FET 23. The diode 31 is connected forward, reverse in direction to the power current flow supplied from  
15 the power line 29 to the energization line 27.

The protection circuit 20 of this embodiment has a first switch (first connection changer) interposed on a connection line between a gate of the FET 23 and a charge pump circuit 25, a first resistor 35 interposed between the gate and the  
20 source of the FET 23, a second resistor 37 interposed between the gate of the FET 23 and the first switch 33, and a second switch (second connection changer) 39 interposed on a connection line 41 between the gate and the source of the FET 23 where the first resistor 35 is interposed. The first and second  
25 switches 33, 39 switch the circuit according to an input control

signal. The second resistor 37 may be interposed between the first switch 33 and the ground, instead of between the FET 23 gate and the first switch 33.

5 The first switch 33 is connected with a connection line leading to the charge pump circuit 25 and a connection line leading to the ground, as viewed from the first switch 33. The both connection lines are to be selectively switched over by the first switch 33 into connection to the gate of the FET 23.

10 The first switch 33 serves also as an on-off switch for the FET 23. When the FET 23 is turned on to drive the load 21, the first switch 33 connects the FET 23 gate to the charge pump circuit 25 (first connection state). Meanwhile, when the FET 23 is turned off to power off the load 21, the first switch 33 connects the FET 23 gate to the ground (second connection state).

15 The second switch 39 is to prevent the gate drive signal outputted from the charge pump circuit 25 from leaking toward the load 21 through the first switch 33 and resistors 35, 37. When the first switch 33 is switched on the charge pump circuit 25, the second switch 39 disconnects the connection line 41 between the gate and the source of the FET 23 where the first resistor 35 is interposed. Meanwhile, when the first switch 33 is switched on the ground side, the second switch 39 puts the connection line 41 in connection.

25 Explanation is now made on the operation of the circuit

arrangement of Fig. 1. During driving the load 21, the first switch 33 is switched on the side of charge pump circuit 25. The gate drive signal outputted from the charge pump circuit 15 is supplied to the FET 23 gate through the first switch 33 and second resistor 37. This allows the power current on the power line 29 to flow to the load 21 through the FET 23, thus driving the load 21. At this time, the second switch 39 puts the connection line 41 in disconnection.

When powering off the load 21, the first switch 33 is switched from the charge pump circuit 25 over to the ground while the second switch 39 puts the connection line in connection. The gate-to-source voltage of FET 23 goes lower than a threshold voltage, to turn off the FET 23 and terminate the energization to the load 21. Due to the turning off of the FET 23, a negative surge is caused by an inductive counter electromotive force on the load 21. This pulls the source voltage of FET 23 toward the minus, to flow a current from the ground toward the load 21 through the first switch 33, second resistor 37, second switch 39 and first resistor 35, as shown by the route P1. At this time, the FET 23 has, between the gate and source, a potential difference of divisional voltage caused in a magnitude commensurate with a source voltage level and a ratio in resistor value of the first and second resistors 35, 37. At a time the gate-to-source voltage exceeds the threshold voltage, the FET 23 turns on. The on-state of FET 23 is held until the

gate-to-source voltage goes below the threshold value. Due to this, during on of the FET 23, the counter electromotive force on the load 21 is absorbed by the power to be supplied from the power line 29 to the load 21 through the FET 23.

5 Meanwhile, the on-state of FET 23 terminates as the negative surge on the load 21 converges and the gate-to-source voltage goes below the threshold value.

Fig. 2 is a figure showing the manner of surge current, etc., during powering off the load 21, in the circuit configuration of Fig. 1. The graph G4 in Fig. 2 shows a change in time of a current  $I_L$  (see Fig. 1) flowing through the load 21 during powering off the load 21 in the circuit arrangement of Fig. 1. The graph G5 shows a change in time of a source voltage  $V_s$  on the FET 23 during powering off the load 21, similarly in the circuit arrangement of Fig. 1. It can be seen from the graph G4, G5 that the protection circuit 20 in this embodiment provides the surge suppression effect nearly equivalent to that of the foregoing protection circuit of Fig. 6.

Herein, in the protection circuit 20 of this embodiment, 20 by adjusting the ratio in resistor value of the first resistor 35 and second resistor 37, it is possible to adjust the gate-to-source voltage of FET 23 caused upon flowing of a current from the ground toward the load 21 through the first and second resistors 35, 37 during occurrence of a negative surge. Due to this, it can be easily adjusted when to turn on the FET 23 25

in what degree the FET 23 source voltage is pulled minus at the occurrence of a negative surge. Furthermore, during occurrence of negative surge, a sufficient level of gate-to-source voltage can be secured (e.g. this can completely turn on the FET 23) at the occurrence of a negative surge. As a result, it is possible to reduce the time T required to absorb negative surge (see Fig. 2).

Fig. 3 is a diagram showing a circuit detailed greater of the protection circuit 20 included in the Fig. 1 circuit arrangement. In Fig. 3 embodiment, N-channel MOS FETs are used as first and second switches 33, 39, as shown in Fig. 3. Also, in this concrete embodiment, the first switch (FET) 33 is interposed between a point 43, between a second resistor 37 and a charge pump circuit 25 on a connection line extending between the FET 23 gate and the charge pump circuit 25, and a ground. The first switch 33 connects and disconnects between the point 43 and the ground, depending upon an input on-off signal. The second switch (FET) 39 similarly connects and disconnects the connection line 41, depending upon the input on-off signal. In this embodiment, the signals for turning on/off the first and second switches 33, 39 and charge pump circuit 25 employ the common on-off signal. Incidentally, in this embodiment, a third resistor 45 is interposed on the connection line extending between the FET 23 gate and the charge pump circuit 25, between the point 43 (point connecting the

first switch 33) and the charge pump 25.

As described above, according to the preset embodiment, a protection circuit 20 can be configured by a simple circuit arrangement using first and second switches 33, 39 and the first and second resistors 35, 37. As a result, while reducing the size and cost of circuit arrangement, countermeasure can be taken to the surge voltage during powering off the load 21 in the circuit arrangement applied with the present embodiment. Moreover, there is no need to use such an element of a Zener diode or the like that possibly generates radio-frequency noise.

Meanwhile, by adjusting the ratio in resistor value of the first resistor 35 and second resistor 37 as in the above, obtained is an effect to reduce the time T required in absorbing a negative surge or the like.

Furthermore, when the first switch 33 is switched on the charge pump circuit 25 to thereby drive the load 21, the second switch 39 disconnects the connection line 41 extending between the gate and the source of the FET 23 where the first resistor 35 is interposed. Accordingly, it is possible to prevent the gate drive signal outputted from the charge pump circuit 25 from leaking toward the load 21 through the connection line 41.

Fig. 4 is a circuit diagram of a protection circuit and circuit arrangement the protection circuit 50 is applied, according to a second embodiment of the present invention. The

circuit arrangement, the protection circuit 50 of this embodiment is applied, has an inductive load (e.g. motor) 51, and an FET 53 as a P-channel MOS transistor for taking control of the energization state to the load 51, as shown in Fig. 4.

5 In this embodiment, the load 51 and the FET 53 are interposed in series on a conductor line 55 such that the FET 53 is located upstream with respect to the direction of power current flow. However, the arrangement may be such that the load 51 is upstream with respect to the direction of current flow. The conductor  
10 line 55 is interposed between the power line 57 and the ground.

The protection circuit 50 of this embodiment has a switch (connection changer) 59 interposed on the connection line between the gate of FET 53 and the ground, a first resistor 61 interposed between the gate of FET 53 and a switch 59, and  
15 a second resistor 63 interposed between the gate and the drain of the FET 53. The switch 59 switches the circuit depending upon an input control signal. The first resistor 61 may be interposed between the switch 59 and the source of FET 53, instead of between the gate of FET 53 and the switch 59.

20 The switch 59 is connected with a connection line leading to the ground and a connection line leading to the source of FET 53, as viewed from the switch 59. The both connection lines can be selectively switched by the switch 59 into connection to the gate of the FET 53.

25 The switch 59 serves also as an on-off switch for the

FET 53. When the FET 53 is turned on to drive the load 51, the switch 59 connects the gate of FET 53 to the ground (first connection state). Meanwhile, when the FET 53 is turned off to power off the load 51, the switch 59 connects the gate of  
5 FET 53 to the source of FET 53 (second connection state).

Explanation is now made on the operation of the circuit arrangement of Fig. 4. During driving the load 51, the switch 59 is switched on the ground. The gate of FET 53 is connected to the ground through the first resistor 61 and switch 59. Due  
10 to this, the gate-to-source voltage of FET 53 exceeds a threshold voltage, to turn on the FET 53. The power current on the power line 57 flows to the load 51 through the FET 53, thereby driving the load 51.

During powering off the load 51, the switch 59 is switched  
15 from the ground over to the source of FET 53. The gate-to-source voltage of FET 53 goes lower than a threshold voltage (once zero substantially), to turn off the FET 53 and terminate the energization to the load 51. Due to turning off of the FET 53, a negative surge is caused by an inductive counter  
20 electromotive force on the load 51. This pulls the gate voltage of FET 53 toward the minus, to flow a current from the source of FET 53 toward the load 51 through the switch 59, the first resistor 61 and the second resistor 63, as shown by the route P2. At this time, the FET 53 at its gate and source has a potential  
25 difference of divisional voltage caused in a magnitude

commensurate with a source-to-drain potential difference level and a ratio in resistor value of the first and second resistors 61, 63. At a time that the gate-to-source voltage exceeds the threshold voltage, the FET 53 turns on. The on-state of FET 53 is held until the gate-to-source voltage goes below the threshold value. Due to this, during on of the FET 53, the counter electromotive force on the load 51 is absorbed by the power to be supplied from the power line 57 to the load 51 through the FET 53. Meanwhile, the on-state of FET 53 terminates as the negative surge by the load 21 converges and the gate-to-source voltage goes below the threshold value.

Herein, in the protection circuit 50 of this embodiment, by adjusting the ratio in resistor value of the first resistor 61 and second resistor 63, it is possible to adjust the gate-to-source voltage of FET 53 caused upon flowing of a current from the source of FET 53 toward the load 51 through the first and second resistors 61, 63 during occurrence of a negative surge. Due to this, it can be easily adjusted whether to turn on the FET 53 in what degree the FET 53 source voltage is pulled minus at the occurrence of a negative surge. Furthermore, when turning on the FET 53 during occurrence of a negative surge, a sufficient level of gate-to-source voltage can be secured (e.g. this can completely turn on the FET 53). As a result, it is possible to reduce the time T required in absorbing a negative surge.

As in the above, according to the present embodiment, a protection circuit 50 can be configured by a simple circuit arrangement using a switch 59 and first and second resistors 61, 63. Accordingly, while reducing the size and cost of circuit arrangement, countermeasure can be taken to a surge voltage upon powering off the load 61 in the circuit arrangement applied with the present embodiment. Moreover, there is no need to use such an element of a Zener diode or the like that possibly generates radio-frequency noise.

10 Also, as in the above, by adjusting the ratio in resistor value of the first resistor 61 and second resistor 62, obtained is an effect to reduce the time required in absorbing negative surge or the like.

Incidentally, the detailed embodiment of circuit arrangement may employ the Fig. 3 FET 33 as a switch 59.

Fig. 5 is a circuit diagram of a protection circuit and circuit arrangement the protection circuit is applied, according to a third embodiment of the present invention. The circuit arrangement, the protection circuit 70 of this embodiment is applied, has an inductive load (e.g. motor) 71, an IGBT 73 for taking control of the energization state to the load 71, and a gate-drive voltage supply source (e.g. drive circuit) for supplying a gate drive voltage for driving the IGBT 73, as shown in Fig. 5. The load 71 and the IGBT 73 are  
25 interposed in series on a conductor line 77 such that the IGBT

73 is located upstream with respect to the direction of power current flow. The conductor line 77 is interposed between the power line 79 and the ground.

The protection circuit 70 of this embodiment has a switch  
5 (connection changer) 81 interposed on the connection line between the gate of IGBT 73 and the gate-drive voltage supply source 75, a first resistor 83 interposed between the gate and the emitter of IGBT 73, and a second resistor 85 interposed between the gate of IGBT 73 and the switch 81. The switch 81  
10 switches the circuit depending upon an input control signal. The second resistor 85 may be interposed between the switch 81 and the ground, instead of between the gate of IGBT 73 gate and the switch 81.

The switch 81 is connected with a connection line leading  
15 to the gate-drive voltage supply source 75 and a connection line leading to the ground, as viewed from the switch 81. The both connection lines can be selectively switched by the switch 81 into connection to the gate of the IGBT 73.

The switch 81 serves also as an on-off switch for the  
20 IGBT 73. When the IGBT 73 is turned on to drive the load 71, the switch 81 connects the gate of IGBT 73 to the gate-drive voltage supply source 75 (first connection state). Meanwhile, when the IGBT 73 is turned off to power off the load 21, the switch 81 connects the gate of IGBT 73 to the ground (second  
25 connection state).

Explanation is now made on the operation of the circuit arrangement of Fig. 5. During driving the load 71, the switch 81 is switched on a side of gate-drive voltage supply source 75. The gate drive voltage outputted from the gate-drive voltage supply source 75 is supplied to the gate of IGBT 73 through the switch 81 and second resistor 85. Due to this, the gate-to-emitter voltage of IGBT 73 exceeds a threshold voltage, to turn on the IGBT 73. The power current on the power line 79 flows to the load 71 through the IGBT 73, thereby driving the load 71.

During powering off the load 71, the switch 81 is switched from the gate-drive voltage supply source 75 over to the ground. The gate of the IGBT 73 is connected to the ground through the second resistor 82 and switch 81, and the gate-to-emitter voltage of IGBT 73 goes lower than a threshold voltage, to turn off the IGBT 73 and terminate the energization to the load 71. Due to turning off of the IGBT 73, a negative surge is caused by an inductive counter electromotive force on the load 71. This pulls the emitter voltage of IGBT 73 toward the minus. As shown by the route P3, a current flows from the ground toward the load 71 through the switch 81 and first and second resistors 83, 85. At this time, the IGBT 73 at its gate and emitter has a potential difference of divisional voltage caused in a magnitude commensurate with an emitter potential level and a resistor value ratio of first and second resistors 83, 85. At

a time that the gate-to-emitter voltage exceeds the threshold voltage, the IGBT 73 turns on. The on-state of IGBT 73 is held until the gate-to-emitter voltage goes below the threshold value. Due to this, during on of the IGBT 73, the counter electromotive  
5 force on the load 71 is absorbed by the power to be supplied from the power line 79 to the load 71 through the IGBT 73. Meanwhile, the on-state of IGBT 73 terminates as the negative surge by the load 71 converges and the gate-to-emitter voltage goes below the threshold value.

10       Herein, in the protection circuit 70 of this embodiment, by adjusting the ratio in resistor value of the first resistor 83 and second resistor 85, it is possible to adjust the gate-to-emitter voltage of IGBT 73 caused upon flowing of a current from the ground toward the load 71 through the first  
15 and second resistors 83, 85 during occurrence of a negative surge. Due to this, it can be easily adjusted when to turn on the IGBT 73 in what degree the IGBT 73 emitter voltage is pulled minus during the occurrence of a negative surge. Furthermore, when turning on the IGBT 73 during the occurrence  
20 of a negative surge, a sufficient level of gate-to-emitter voltage can be secured (e.g. this can completely turn on the IGBT 73). As a result, it is possible to reduce the time required for absorbing negative surge.

As described above, according to the preset embodiment,  
25 a protection circuit 70 can be configured by a simple circuit

arrangement using a switch 81 and first and second resistors 83, 85. Accordingly, while reducing the size and cost of circuit arrangement, countermeasure can be taken to the surge voltage during powering off the load 71 in the circuit arrangement applied with the present embodiment. Moreover, there is no need to use such an element of a Zener diode or the like that possibly generates radio-frequency noise.

Also, as described above, by adjusting the ratio in resistor value of the first resistor 83 and second resistor 85, obtained is an effect to reduce the time required for absorbing negative surge or so.

Incidentally, the detailed embodiment of circuit arrangement may use the FET 33 of Fig. 3 as the switch 81.

According to an aspect of the invention, during powering off the load, the first connection changer is changed from a first connection state the gate of an FET is connected to a gate drive voltage supply source to a second connection state the gate is connected to the ground. By a negative surge caused due to powering off the load, the gate-to-source voltage of FET exceeds a threshold and the FET turns from off to on whereby a negative surge can be absorbed by a current flowing to the load through the FET. Accordingly, a protection circuit can be configured by a simple circuit arrangement. As a result, while reducing the size and cost of circuit arrangement, countermeasure can be taken to the surge voltage during powering

off the load in the circuit arrangement applied with the present embodiment. Moreover, there is no need to use such an element of a Zener diode or the like that possibly generates radio-frequency noise.

5       According to another aspect of the invention, by adjusting the ratio in resistor value of the first resistor and second resistor, it is possible to adjust the FET gate-to-source voltage caused upon flowing of a current from the ground to the FET source through the first and second resistors at the occurrence  
10 of a negative surge. Due to this, it is possible to easily adjust whether to turn on the FET in what degree the FET source voltage is pulled toward the minus upon occurrence of a negative surge occurrence. Furthermore, a sufficient level of gate-to-source voltage can be obtained in turning on the FET  
15 upon occurrence of a surge (e.g. this can turn on the FET completely). As a result, it is possible to reduce the time required in absorbing the surge.

      According to another aspect of the invention, the first connection changer is placed in a first connection state the  
20 FET gate is connected to the gate drive voltage supply source, to turn on the FET. In the case the load is being driven, the second switch disconnects the connection line between the gate and the source of the FET, thereby making it possible to prevent the gate drive signal outputted from the gate drive voltage  
25 supply source from leaking toward the load through the first

resistor.

According to yet another aspect of the invention, during powering off the load, the connection changer is changed from a first connection state the gate of FET is connected to the ground to a second connection state the gate is connected to the source. Due to this, the gate-to-source voltage of FET, caused by a current flow from the FET source to the drain through the connection changer and first and second resistors, exceeds a threshold due to a surge occurrence by powering off the load, thereby turning the FET from off to on whereby a surge can be absorbed by a current flow to the load. Accordingly, a protection circuit can be configured by a simple circuit arrangement. As a result, while reducing the size and cost of circuit arrangement, countermeasure can be taken to the surge voltage during powering off the load in the circuit arrangement applied with the present embodiment. Moreover, there is no need to use such an element of a Zener diode or the like that possibly generates radio-frequency noise.

Also, by adjusting the ratio in resistor value of the first resistor and second resistor, it is possible to adjust the FET gate-to-source voltage caused upon flowing of a current from the FET source to the ground through the first and second resistors upon occurrence of a surge. Due to this, it is possible to easily adjust whether to turn on the FET in what magnitude a surge is caused. Furthermore, a sufficient level of

gate-to-source voltage can be obtained in turning on the FET upon occurrence of a surge (e.g. this can turn on the FET completely). As a result, it is possible to reduce the time required for absorbing the surge.

5       According to still another aspect of the invention, during powering off the load, the connection changer is changed from a first connection state the gate of IGBT is connected to a gate drive voltage supply source to the second connection state the gate is connected to a ground. The gate-to-emitter voltage  
10 of IGBT exceeds a threshold due to the occurrence of a negative surge by powering off the load, thereby turning the IGBT from off to on whereby a negative surge can be absorbed by a current flow to the load through the IGBT. Accordingly, a protection circuit can be configured by a simple circuit arrangement. As  
15 a result, while reducing the size and cost of circuit arrangement, countermeasure can be taken to the surge voltage during powering off the load in the circuit arrangement applied with the present embodiment. Moreover, there is no need to use such an element of a Zener diode or the like that possibly generates  
20 radio-frequency noise.

      According to yet another aspect of the invention, by adjusting the ratio in resistor value of the first resistor and second resistor, it is possible to adjust the IGBT gate-to-emitter voltage caused upon flowing of a current from  
25 the ground to the IGBT emitter through the first and second

resistors upon occurrence of a negative surge. Due to this, it is possible to easily adjust whether to turn on the FET in what degree the IGBT emitter voltage is pulled toward the minus upon occurrence of a negative surge. Furthermore, a sufficient  
5 level of gate-to-emitter voltage can be obtained in turning on the IGBT upon occurrence of a negative surge (e.g. this can turn on the IGBT completely). As a result, it is possible to reduce the time required in absorbing the negative surge.